NCP380

Fixed / Adjustable Current-Limiting Power-Distribution Switches

The NCP380 is a high side power−distribution switch designed for applications where heavy capacitive loads and short−circuits are likely to be encountered. The device includes an integrated 55 mΩ (DFN package), P−channel MOSFET. The device limits the output current to a desired level by switching into a constant−current regulation mode when the output load exceeds the current−limit threshold or a short is present. The current−limit threshold is either user adjustable between 100 mA and 2.1 A via an external resistor or internally fixed. The power−switch rise and fall times are controlled to minimize current ringing during switching.

An internal reverse−voltage detection comparator disables the power−switch if the output voltage is higher than the input voltage to protect devices on the input side of the switch.

The $\overline{\text{FLAG}}$ logic output asserts low during over current, reverse−voltage or over temperature conditions. The switch is controlled by a logic enable input active high or low.

Features

- 2.5 V – 5.5 V Operating Range
- 70 mΩ High−Side MOSFET
- Current Limit:
  - User adjustable from 100 mA to 2.1 A
  - Fixed 500 mA, 1 A, 1.5 A, 2 A and 2.1 A
- Under Voltage Lock−out (UVLO)
- Built−in Soft−start
- Thermal Protection
- Soft Turn−off
- Reverse Voltage Protection
- Junction Temperature Range: −40°C to 125°C
- Enable Active High or Low (EN or $\overline{\text{EN}}$)
- Compliance to IEC61000−4−2 (Level 4)
  - 8.0 kV (Contact)
  - 15 kV (Air)
- Certified UL CB Schem
- Pb−Free Packages are Available

Typical Applications

- Laptops
- USB Ports/Hubs
- TVs

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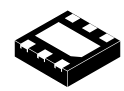
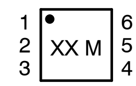
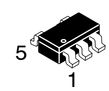
MARKING DIAGRAMS

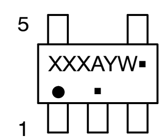


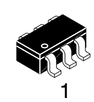
UDFN6
MU SUFFIX
CASE 517AB



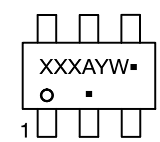


TSOP−5
SN SUFFIX
CASE 483





TSOP−6
SN SUFFIX
CASE 318G

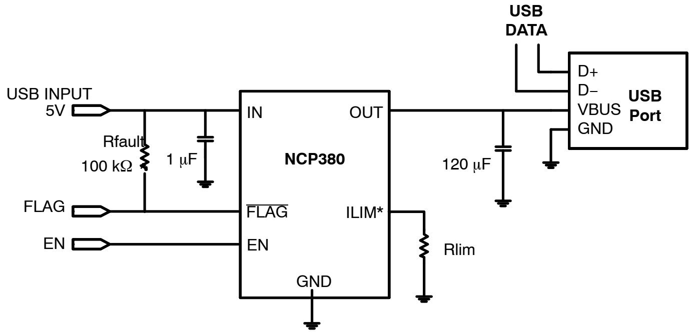


XXX = Specific Device Code
A =Assembly Location
M = Date Code
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.



*For adjustable version only.

Figure 1. Typical Application Circuit

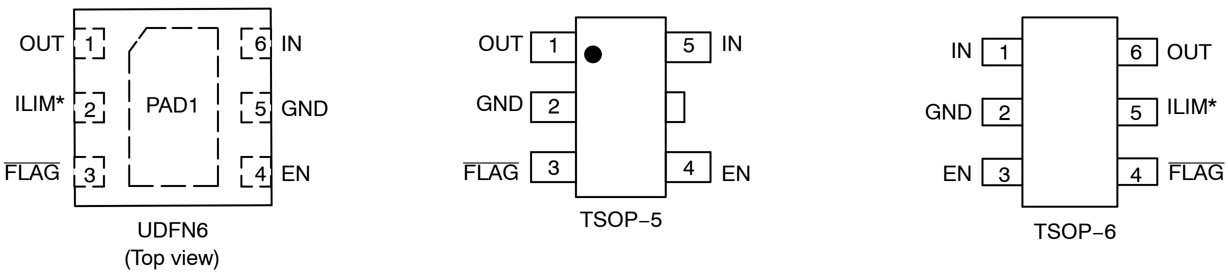


Figure 2. Pin Connections

*For adjustable version only, otherwise not connected.

PIN FUNCTION DESCRIPTION

Pin Name	Type	Description
EN	INPUT	Enable input, logic low/high (i.e. $\overline{EN}$ or EN) turns on power switch
GND	POWER	Ground connection;
IN	POWER	Power−switch input voltage; connect a 1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
$\overline{FLAG}$	OUTPUT	Active−low open−drain output, asserted during overcurrent, overtemperature or reverse−voltage conditions. Connect a 10 kΩ or greater resistor pull−up, otherwise leave unconnected.
OUT	OUTPUT	Power−switch output; connect a 1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended. A 1 μF or greater ceramic capacitor from OUT to GND must be connected if the USB requirement (i.e.120 μF capacitor minimum) is not met.
ILIM*	INPUT	External resistor used to set current−limit threshold; recommended 5 kΩ < R_{ILIM} < 250 kΩ.
PAD1**	THERMAL	Exposed Thermal Pad: Must be soldered to PCB Ground plane

*(For adjustable version only, otherwise not connected.
**For DFN version only.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
From IN to OUT Pins: Input/Output (Note 1)	V_{IN} , V_{OUT}	−7.0 to +7.0	V
IN, OUT, EN, ILIM, $\overline{FLAG}$, Pins: Input/Output (Note 1)	V_{EN}, V_{ILIM}, V_{FLAG}, V_{IN}, V_{OUT}	−0.3 to +7.0	V
$\overline{FLAG}$ sink current	I_{SINK}	1	mA
I_{LIM} source current	I_{LIM}	1	mA
ESD Withstand Voltage (IEC 61000−4−2) (output only, when bypassed with 1.0 μF capacitor minimum)	ESD IEC	15 Air, 8 contact	kV
Human Body Model (HBM) ESD Rating (Note 2)	ESD HBM	2000	V
Machine Model (MM) ESD Rating (Notes 2 and 3)	ESD MM	200	V
Latch−up protection (Note 4) − Pins IN, OUT, EN, ILIM, $\overline{FLAG}$	LU	 100	mA
Maximum Junction Temperature Range (Note 6)	T_J	−40 to +TSD	°C
Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
3. Except EN pin, 150 V.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.
6. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.

OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			2.5		5.5	V
V_{EN}	Enable Voltage			0		5.5	
T_A	Ambient Temperature Range			−40	25	+85	°C
T_J	Junction Temperature Range			−40	25	+125	°C
R_{ILIM}	Resistor from ILIM to GND pin			5.0		250	kΩ
I_{SINK}	$\overline{\text{FLAG}}$ sink current					1.0	mA
C_{IN}	Decoupling input capacitor			1.0			μF
C_{OUT}	Decoupling output capacitor	USB port per Hub		120			μF
$R_{\theta JA}$	Thermal Resistance Junction−to−Air	UDFN−6 package (Notes 7 and 8)			120		°C/W
		TSOP−5 package (Notes 7 and 8)			305		°C/W
		TSOP−6 package (Notes 7 and 8)			280		°C/W
I_{OUT}	Maximum DC current	UDFN−6 package				2.1	A
		TSOP−5, TSOP−6 package				1.0	A
P_D	Power Dissipation Rating (Note 9)	$T_A \leq 25°C$	UDFN−6 package		830		mW
			TSOP−5 package		325		mW
			TSOP−6 package		350		mW
		$T_A = 85°C$	UDFN−6 package		325		mW
			TSOP−5 package		130		mW
			TSOP−6 package		145		mW

7. A thermal shutdown protection avoids irreversible damage on the device due to power dissipation.
8. The $R_{\theta JA}$ is dependent of the PCB heat dissipation. Board used to drive this data was a 2” x 2” NCP380EVB board. It is a 2 layers board with 2−once copper traces on top and bottom of the board. Exposed pad is connected to ground plane for UDFN−6 version only.
9. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 2.5 V to 5.5V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 5 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
$R_{DS(on)}$	Static drain−source on−state resistance DFN Package	V_{IN} = 5 V	−40°C < T_J < 125°C		55	75	mΩ
			−40°C < T_J < 125°C			110	
	TSOP Package	V_{IN} = 5 V	−40°C < T_J < 125°C		70	95	mΩ
			−40°C < T_J < 125°C			135	
T_R	Output rise time	V_{IN} = 5 V	C_{LOAD} = 1 μF, R_{LOAD} = 100 Ω (Note 10)	0.3	1.0	1.5	ms
		V_{IN} = 2.5 V		0.2	0.65	1.0	
T_F	Output fall time	V_{IN} = 5 V		0.1		0.5	
		V_{IN} = 2.5 V		0.1		0.5	
ENABLE INPUT EN OR $\overline{EN}$							
V_{IH}	High−level input voltage			1.2			V
V_{IL}	Low−level input voltage					0.4	V
I_{EN}	Input current	V_{EN} = 0 V, $V_{\overline{EN}}$ = 5 V		−0.5		0.5	μA
T_{ON}	Turn on time	C_{LOAD} = 1 μF, R_{LOAD} = 100 Ω (Note 11)		2.0	3.0	4.0	ms
T_{OFF}	Turn off time			1.0		3.0	ms
CURRENT LIMIT							
I_{OCP}	Current−limit threshold (Maximum DC output current I_{OUT} delivered to load)	V_{IN} = 5 V	R_{ILIM} = 20 kΩ (Note 11)	950	1200	1450	mA
			R_{ILIM} = 40 kΩ (Note 11)	550	700	850	
			Fixed 0.5 A (Note 12)	0.5	0.58	0.65	A
			Fixed 1.0 A (Note 12)	1.0	1.15	1.3	
			Fixed 1.5 A (Note 12)	1.5	1.75	1.9	
			Fixed 2.0 A (Note 12)	2.0	2.25	2.5	
			Fixed 2.1 A (Note 12)	2.1	2.25	2.5	
T_{DET}	Response time to short circuit	V_{IN} = 5 V			2.0		μs
T_{REG}	Regulation time			1.8	3.0	4.0	ms
T_{OCP}	Overcurrent protection time			14	20	26	ms
REVERSE−VOLTAGE PROTECTION							
V_{REV}	Reverse−voltage comparator trip point ($V_{OUT} - V_{IN}$)				100		mV
T_{REV}	Time from reverse−voltage condition to MOSFET switch off & $\overline{FLAG}$ low	V_{IN} = 5 V		4.0	6.0	9.0	ms
T_{RREV}	Re−arming Time			7.0	10	15	ms
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	IN pin low−level input voltage	V_{IN} rising		2.0	2.3	2.4	V
V_{HYST}	IN pin hysteresis	T_J = 25°C		25		60	mV
T_{RUVLO}	Re−arming Time			7.0	10	15	ms
SUPPLY CURRENT							
I_{INOFF}	Low−level output supply current.	V_{IN} = 5 V, No load on OUT, Device OFF V_{EN} = 0 V or $V_{\overline{EN}}$ = 5 V			1.0	2.1	μA
I_{INON}	High−level output supply current.	V_{IN} = 5 V, device enable 2 A version 1 A and 1.5 A current version 0.5 A current version				 90 80 70	μA

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C and T_J up to + 125°C for V_{IN} between 2.5 V to 5.5V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and V_{IN} = 5 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SUPPLY CURRENT							
I_{REV}	Reverse leakage current	V_{OUT} = 5 V, V_{IN} = 0 V	T_J = 25°C			1.0	μA
$\overline{FLAG}$ PIN							
V_{OL}	$\overline{FLAG}$ output low voltage	$I_{\overline{FLAG}}$ = 1 mA				400	mV
I_{LEAK}	Off−state leakage	$V_{\overline{FLAG}}$ = 5 V				1.0	μA
T_{FLG}	$\overline{FLAG}$ deglitch	$\overline{FLAG}$ de−assertion time due to overcurrent or reverse voltage condition		4.0	6.0	9.0	ms
T_{FOCP}	$\overline{FLAG}$ deglitch	$\overline{FLAG}$ assertion due to overcurrent		6.0	8.0	12	ms
THERMAL SHUTDOWN							
T_{SD}	Thermal shutdown threshold				140		°C
T_{SDOCP}	Thermal regulation threshold				125		°C
T_{RSD}	Thermal shutdown rearming threshold				115		°C

10. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground, See Figure 3.
11. Adjustable current version, R_{ILIM} tolerance ±1%.
12. Fixed current version.

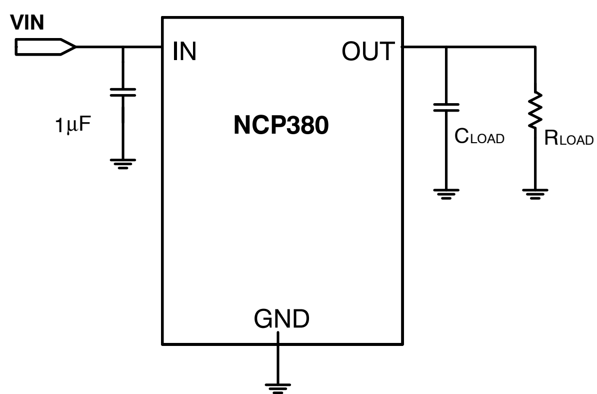


Figure 3. Test Configuration

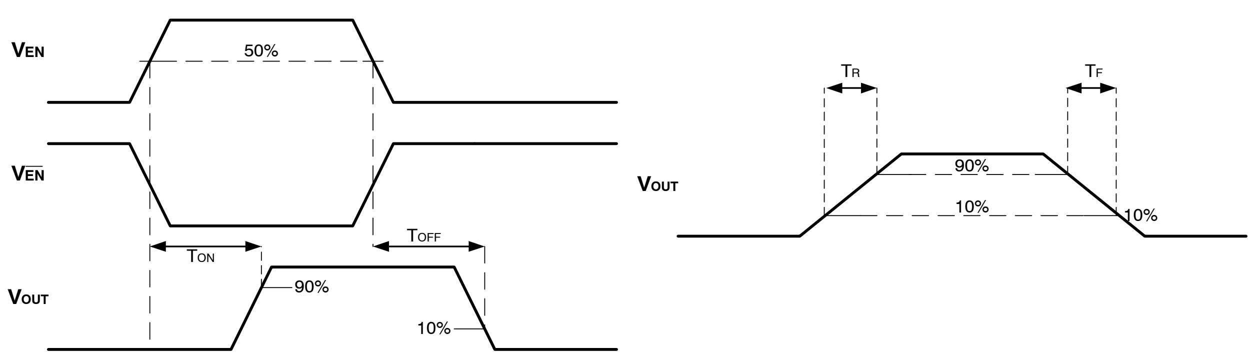


Figure 4. Voltage Waveform

BLOCK DIAGRAM

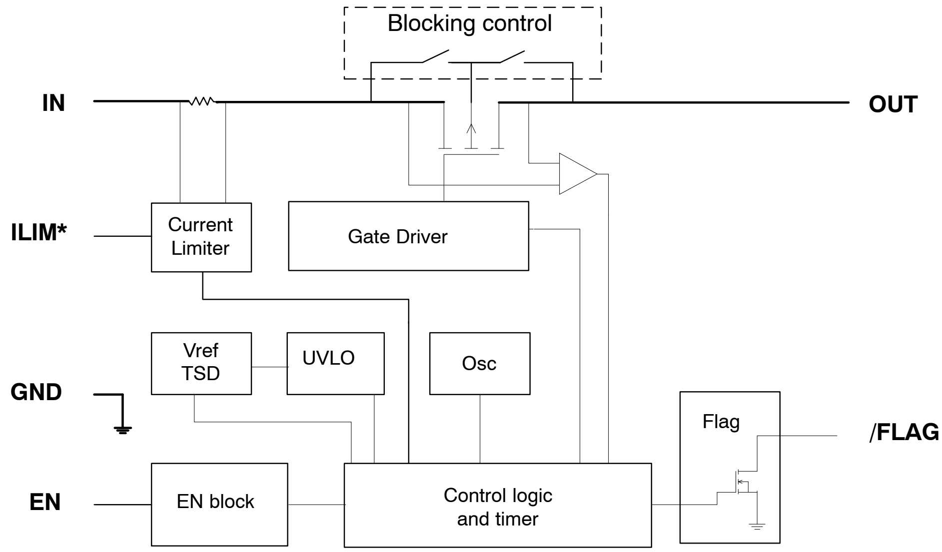


Figure 5. Block Diagram

*For adjustable version only, otherwise not connected.

FUNCTIONAL DESCRIPTION

Overview

The NCP380 is a high side P channel MOSFET power distribution switch designed to protect the input supply voltage in case of heavy capacitive loads, short circuit or over current. In addition, the high side MOSFET is turned off during under voltage, thermal shutdown or reverse voltage condition. Adjustable version allows the user to program the current limit threshold using an external resistor. Thanks to the soft start circuitry, NCP380 is able to limit large current and voltage surges.

Overcurrent Protection

NCP380 switches into a constant current regulation mode when the output current is above the I_{OCP} threshold. Depending on the load, the output voltage is decreased accordingly.

- In case of hot plug with heavy capacitive load, the output voltage is brought down to the capacitor voltage. The NCP380 will limit the current to the I_{OCP} threshold value until the charge of the capacitor is completed.

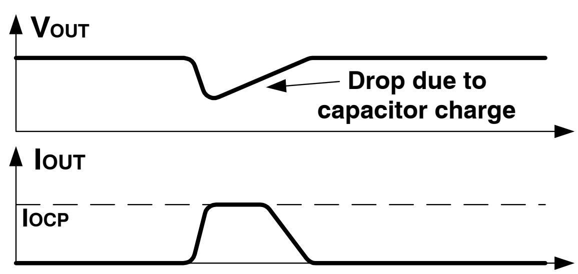


Figure 6. Heavy capacitive load

- In case of overload, the current is limited to the I_{OCP} value and the voltage value is reduced according to the load by the following relation:

$$V_{OUT} = R_{LOAD} \times I_{OCP} \qquad \text{(eq. 1)}$$

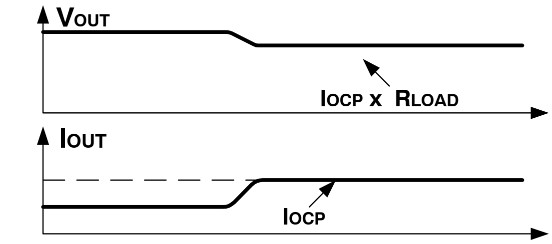


Figure 7. Overload

– In case of short circuit or huge load, the current is limited to the I_{OCP} value within T_{DET} time until the short condition is removed. If the output remains shorted or tied to a very low voltage, the junction temperature of the chip exceeds T_{SDOCP} value and the device enters in thermal shutdown (MOSFET is turned−off).

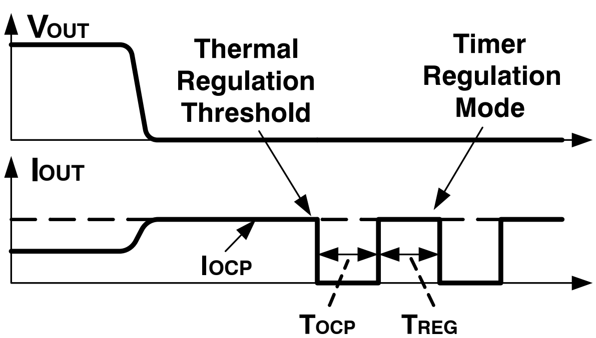


Figure 8. Short circuit

Then, the device enters in timer regulation mode, described in 2 phases:

– Off−phase: Power MOSFET is off during T_{OCP} to allow the die temperature to drop.
– On−phase: regulation current mode during $T_{REG.}$ The current is regulated to the I_{OCP} level.

The timer regulation mode allows the device to handle high thermal dissipation (in case of short circuit for example) within temperature operating condition.

NCP380 stays in on−phase/off−phase loop until the over current condition is removed or enable pin is toggled.

Remark: other regulation modes can be available for different applications. Please contact our On Semiconductor representative for availability.

$\overline{\text{FLAG}}$ Indicator

The $\overline{\text{FLAG}}$ pin is an open−drain MOSFET asserted low during over current, reverse−voltage or over temperature conditions. When an over current or a reverse voltage fault is detected on the power path, $\overline{\text{FLAG}}$ pin is asserted low at the end of the associate deglitch time (see electrical characteristics). Thanks to this feature, the $\overline{\text{FLAG}}$ pin is not tied low during the charge of a heavy capacitive load or a voltage transient on output. Deglitch time is T_{FOCP} for over current fault and T_{REV} for reverse voltage. The $\overline{\text{FLAG}}$ pin remains low until the fault is removed. Then, the $\overline{\text{FLAG}}$ pin goes high at the end of T_{FGL}.

Undervoltage Lock−out

Thanks to a built−in under voltage lockout (UVLO) circuitry, the output remains disconnected from input until V_{IN} voltage is below V_{UVLO}. When V_{IN} voltage is above V_{UVLO}, the system try to reconnect the output after a rearming time. T_{RUVLO}. This circuit has a V_{HYST} hysteresis witch provides noise immunity to transient.

Thermal Sense

Thermal shutdown turns off the power MOSFET if the die temperature exceeds T_{SD}. A Hysteresis prevents the part from turning on until the die temperature cools at $T_{RSD.}$

Reverse Voltage Protection

When the output voltage exceeds the input voltage by V_{REV} voltage during T_{REV}, the reverse voltage circuitry disconnects the output in order to protect the power supply. The same time T_{REV} is needed to turn on again the power MOS plus a rearming time T_{RREV}.

Enable Input

Enable pin must be driven by a logic signal (CMOS or TTL compatible) or connected to the GND or VIN. A logic low on $\overline{\text{EN}}$ or high on EN turns−on the device. A logic high on $\overline{\text{EN}}$ or low on EN turns off device and reduces the current consumption down to I_{INOFF}.

Blocking Control

The blocking control circuitry switches the bulk of the power MOS. When the part is off, the body diode limits the leakage current I_{REV} from OUT to IN. In this mode, anode of the body diode is connected to IN pin and cathode is connected to OUT pin. In operating condition, anode of the body diode is connected to OUT pin and cathode is connected to IN pin preventing the discharge of the power supply.

APPLICATION INFORMATION

Power Dissipation

The junction temperature of the device depends on different contributing factors such as board layout, ambient temperature, device environment, etc... Yet, the main contributor in terms of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$R_D = R_{DS(on)} \times \left(I_{OUT}\right)^2 \qquad \text{(eq. 2)}$$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

$$T_J = P_D \times R_{\theta JA} + T_A \qquad \text{(eq. 3)}$$

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

Power dissipation in regulation mode can be calculated by taking into account the drop $V_{IN} - V_{OUT}$ link to the load by the following relation:

$$P_D = \left(V_{IN} - R_{LOAD} \times I_{OCP}\right) \times I_{OCP} \qquad \text{(eq. 4)}$$

P_D = Power dissipation (W)
V_{IN} = Input Voltage (V)
R_{LOAD} = Load Resistance (Ω)
I_{OCP} = Output regulated current (A)

Adjustable Current−Limit Programming (For adjustable version only)

The R_{LIM} resistor connected between ILIM pin and GND determines the current limit threshold according to the following curve.

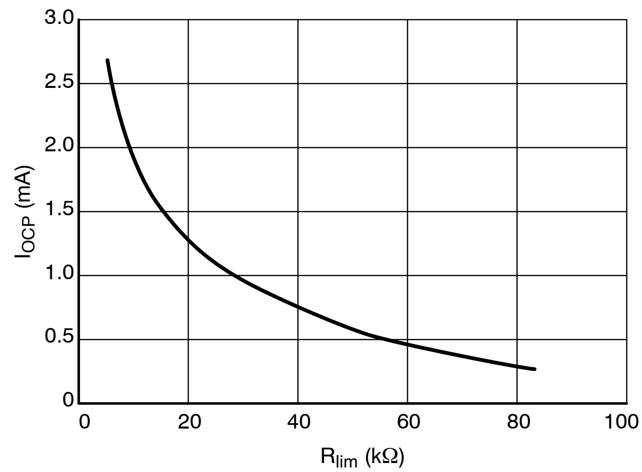


Figure 9. I_{OCP} versus R_{lim}

To ensure system stability, R_{ILIM} resistor must be connected as close as possible to the IC and the maximum recommended value is 250 kΩ

PCB Recommendations

The NCP380 integrates a PMOS FET rated up to 2 A, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. The UDFN6 PAD1 must be connected to ground plane to increase the heat transfer if necessary. This pad must be connected to ground plane. By increasing PCB area, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

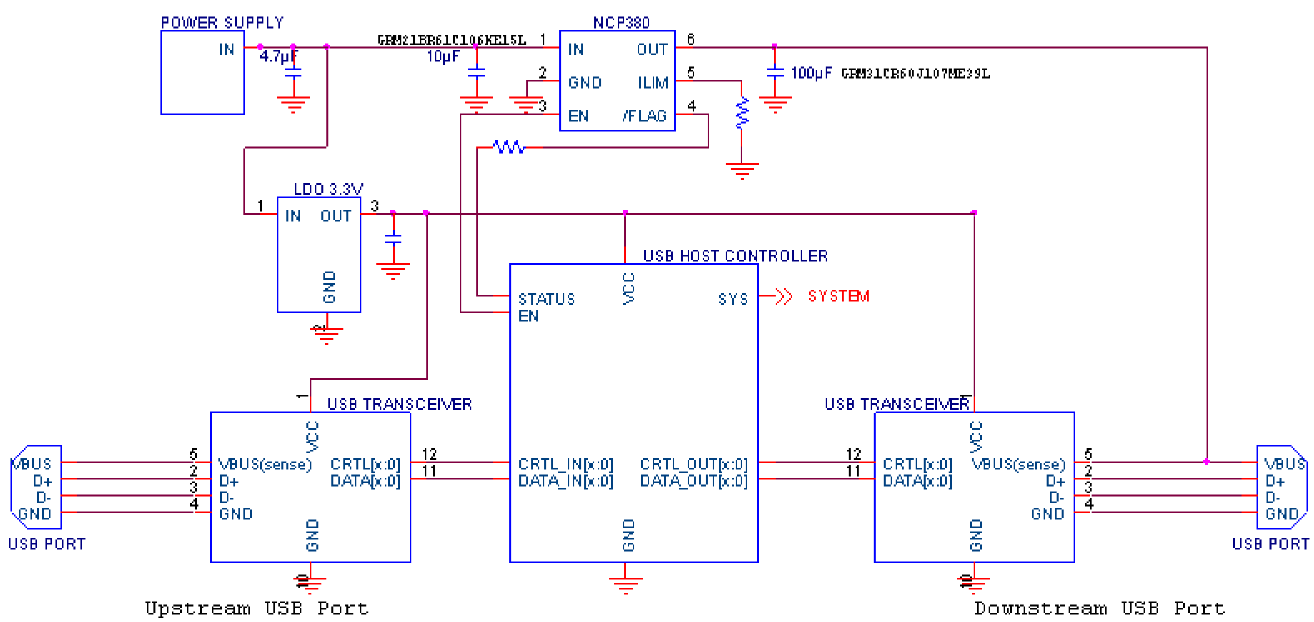


Figure 10. USB Host Typical Application

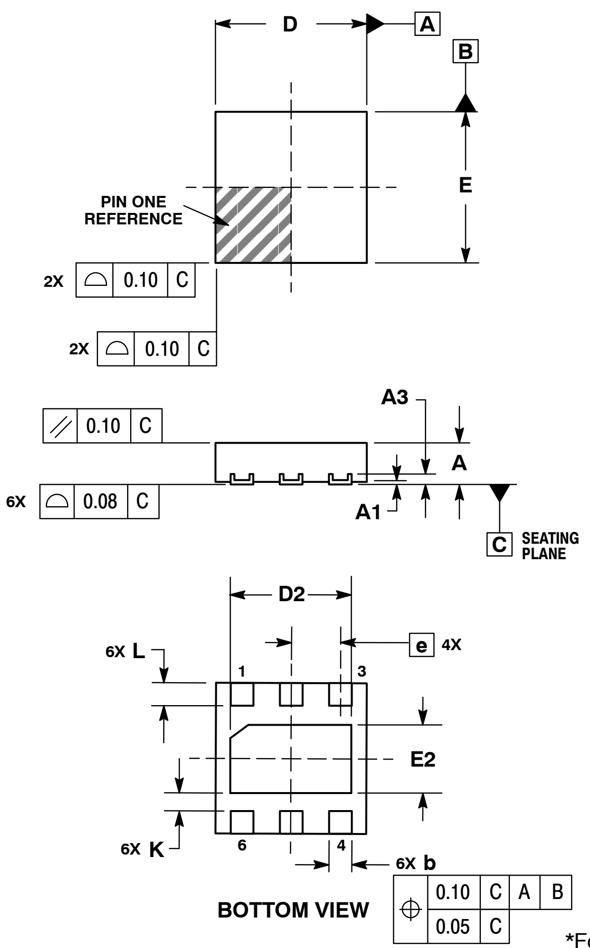
ORDERING INFORMATION

Device	Marking	Active Enable Level	Over Current Limit	Evaluation Board	Package	Shipping†
NCP380LSNAJAAT1G	AAC	Low	Adjustable	NCP380LSNAJAGEVB	TSOP−6 (Pb−Free)	3000 Tape / Reel
NCP380LSN05AAT1G	AC5		500 mA	NCP380LSN05AGEVB	TSOP−5 (Pb−Free)	
NCP380LSN10AAT1G	AC6		1 A	NCP380LSN10AGEVB		
NCP380LMUAJAATBG	AA		Adjustable	NCP380LMUAJAGEVB	UDFN6 (Pb−Free)	
NCP380LMU05AATBG	AE		500 mA	NCP380LMU05AGEVB		
NCP380LMU10AATBG	AF		1 A	NCP380LMU10AGEVB		
NCP380LMU15AATBG	AG		1.5 A	NCP380LMU15AGEVB		
NCP380LMU20AATBG	AL		2 A	NCP380LMU20AGEVB		
NCP380HSNAJAAT1G	AAD	High	Adjustable	NCP380HSNAJAGEVB	TSOP−6 (Pb−Free)	
NCP380HSN05AAT1G	AC7		500 mA	NCP380HSN05AGEVB	TSOP−5 (Pb−Free)	
NCP380HSN10AAT1G	ADA		1 A	NCP380HSN10AGEVB		
NCP380HMUAJAATBG	AC		Adjustable	NCP380HMUAJAGEVB	UDFN6 (Pb−Free)	
NCP380HMU05AATBG	AH		500 mA	NCP380HMU05AGEVB		
NCP380HMU10AATBG	AJ		1 A	NCP380HMU10AGEVB		
NCP380HMU15AATBG	AK		1.5 A	NCP380HMU15AGEVB		
NCP380HMU20AATBG	AM		2 A	NCP380HMU20AGEVB		
NCP380HMU21AATBG	AU		2.1 A	NCP380HMU21AGEVB		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

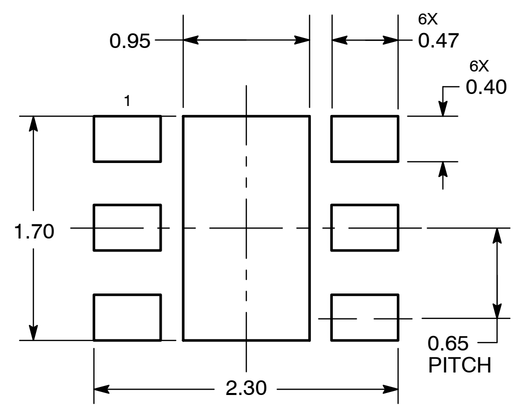
UDFN6 2x2, 0.65P
CASE 517AB−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
K	0.20	---
L	0.25	0.35

SOLDERING FOOTPRINT*

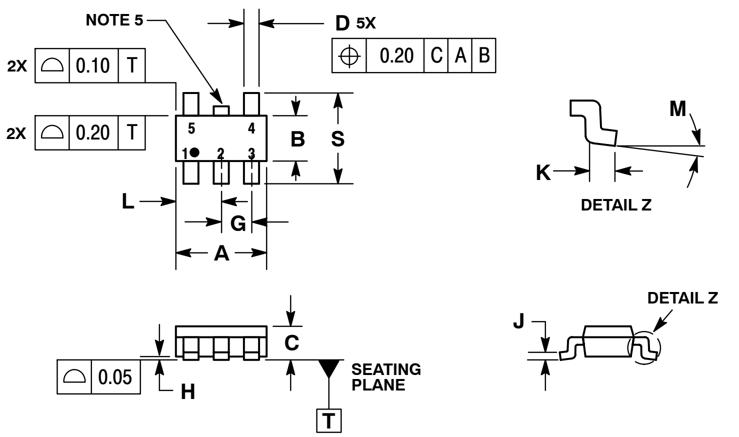


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

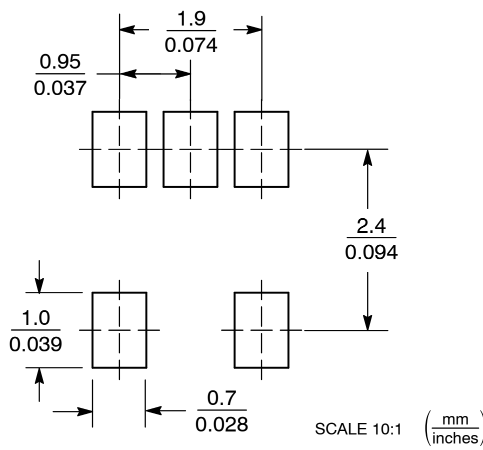
TSOP−5
CASE 483−02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

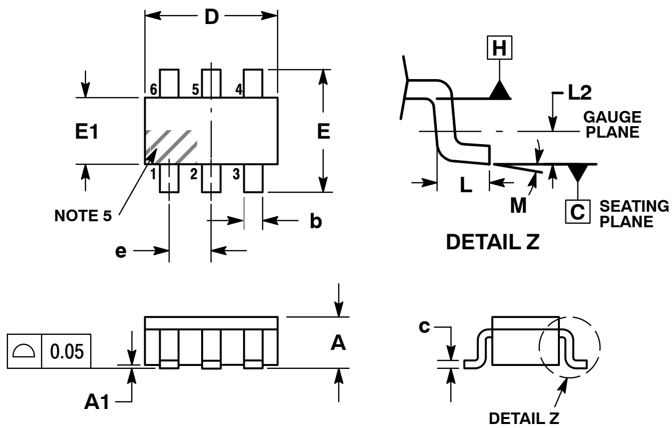
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

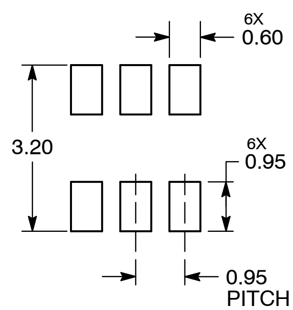
TSOP−6
CASE 318G−02
ISSUE U



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2		0.25 BSC	
M	0°	−	10°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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